WHAT IS CLAIMED IS:

1. A semiconductor apparatus comprising a semiconductor device, an electrically insulating layer having an inclined portion and formed on said semiconductor device by printing an electrically insulating material by use of a mask, an external connection terminal formed on said electrically insulating layer, and wiring formed on said electrically insulating layer for electrically connecting said external connection terminal with a circuit electrode of said semiconductor device.

2. A semiconductor apparatus according to Claim 1, wherein said electrically insulating layer has particles.

3. A semiconductor apparatus comprising a semiconductor device; an electrically insulating layer containing particles, having an inclined portion and formed on said semiconductor device; an external connection terminal formed on said electrically insulating layer; and wiring formed on said electrically insulating layer for electrically connecting said external connection terminal with a circuit electrode of said semiconductor device.

4. A semiconductor apparatus according to Claim 2 or 3, wherein said particles are made of the same material as said electrically insulating material of said electrically insulating layer.

5. A semiconductor apparatus according to Claim

2 or 3, wherein said particles contained in said electrically insulating layer are formed so that a size of said particles near said semiconductor device is larger than a size of said particles near said external connection terminal.

6. A semiconductor apparatus according to Claim 2 or 3, wherein a size of said particles is not larger than 10 micrometers.

7. A semiconductor apparatus according to Claim 1 or 3, wherein a lump portion is provided in a vicinity of a boundary between said inclined portion of said electrically insulating layer and a flat portion of said electrically insulating layer having an approximately uniform thickness.

8. A semiconductor apparatus according to Claim 1 or 3, wherein a thickness of said electrically insulating layer is in a range of from about 35 to about 150 micrometers.

9. A semiconductor apparatus according to Claim 1 or 3, wherein a thickness of said electrically insulating layer is in a range of from 1/20 to 1/5 as large as thickness of said semiconductor device.

10. A semiconductor apparatus according to Claim 1 or 3, wherein the inclined portion of said electrically insulating layer is inclined at a gradient in a range of from about 5% to about 30% with respect to a circuit surface of said semiconductor device.

11. A semiconductor apparatus according to Claim

1 or 3, wherein an elastic modulus of said electrically insulating layer is in a range of from about 0.1 GPa to about 10 GPa.

12. A semiconductor apparatus according to Claim 1 or 3, wherein said electrically insulating layer is made of a material curable at a temperature in a range of from about 100℃ to about 250℃.

13. A semiconductor apparatus according to Claim 1 or 3, wherein a glass degradation temperature of said electrically insulating layer is in a range of from 150℃ to 400℃.

14. A semiconductor apparatus according to Claim 1 or 3, wherein a heat degradation temperature of said electrically insulating layer is in a range of from 300℃ to 450℃.

15. A semiconductor apparatus comprising a semiconductor device, an electrically insulating layer formed on said semiconductor device, and a wiring formed on said electrically insulating layer and provided for electrically connecting an external connection terminal formed on said electrically insulating layer with a circuit electrode of said semiconductor device, wherein:

a glass transition temperature of said electrically insulating layer is in a range of from 150℃ to 400℃; and

a heat degradation temperature of said electrically insulating layer is in a range of from

300℃ to 450℃.

16. A semiconductor apparatus according to Claim 1 or 3, wherein said electrically insulating layer is made of at least one member selected from the group consisting of polyimide, polyamide, polyamide-imide, epoxy, phenol, and silicone.

17. A semiconductor apparatus according to Claim 1 or 3, wherein said electrically insulating layer has characteristic which varies in accordance with a direction of thickness thereof so that the characteristic of said electrically insulating layer at a semiconductor device side is near characteristic of said semiconductor device and the characteristic of an external connection terminal-side portion of said electrically insulating layer is near the characteristic of a substrate on which said semiconductor device is mounted.

18. A semiconductor apparatus according to Claim 1 or 3, wherein said electrically insulating layer has characteristic which changes in accordance with a direction of thickness thereof so that thermal expansion coefficient of said electrically insulating layer decreases as a position of said electrically insulating layer goes from said external connection terminal toward said semiconductor device.

19. A method for producing a semiconductor apparatus comprising a step of forming an electrically insulating layer on a wafer by printing by use of a

mask.

20. A method for producing a semiconductor apparatus comprising:

a first step of forming an electrically insulating layer on a wafer by printing by use of a mask;

a second step of forming a wiring over an area from a circuit electrode of said wafer to an inclined portion and a flat portion of said electrically insulating layer; and

a third step of forming an external connection terminal on said electrically insulating layer so that said external connection terminal is electrically connected with said circuit electrode through said wiring.

21. A method for producing a semiconductor apparatus comprising:

a first step of forming an electrically insulating layer on a wafer by printing by use of a mask;

a second step of forming a pad on said electrically insulating layer;

a third step of forming a wiring on said electrically insulating layer so that said wiring electrically connects a circuit electrode of said wafer with said pad; and

a fourth step of forming an external connection terminal on said pad.

22. A method for producing a semiconductor apparatus according to any one of Claims 19 through 21, wherein said electrically insulating layer contains particles.

23. A method for producing a semiconductor apparatus according to any one of Claims 19 through 21, wherein said electrically insulating layer is formed by repeating printing by a plurality of times by use of said mask.

24. A method for producing a semiconductor apparatus according to any one of Claims 19 through 21, wherein said first step of forming said electrically insulating layer by printing is performed in a manner so that a squeegee is moved over an opening portion of said mask from a vertex to an opposite vertex.